Profile of Faculty

Name	G.BALA KISHORE
Designation	Assistant professor
Department	Electronics & Communication Engineering
Date of Birth	06/07/1987
AICTE Unique ID	1-2978208615
Education Qualifications	B.Tech (ECE), M.Tech (DECS)
Work Experience	B.Tech (ECE), W.Tech (DECS)
Teaching	11 YEARS
Research	-
Industry	_
others	-
Area of Specialization	Digital Electronics & Communication systems
Courses taught at Diploma/ Post Diploma/	Diploma: Electronics Circuits, Digital Electronics, Optical
Under Graduate/ Post Graduate/ Post Graduate Diploma level	Mobile Communications, IMST, Linear integrated Circuits, UG: Electronic Devices & Circuits, , Electronic Circuit Analysis, Linear integrated Circuits, DSD through HDL, Digital Signal Processing, Optical Communication, Cellular Mobile Communication PG:DSP Architecture, Embedded system Design, Digital System Design
Research guidance (Number of Students)	UG: 10 Batches, PG: 4
No. of papers published in National/	National Journals – 1
International Journals/ Conferences	International Journals – 1
Master (Completed/Ongoing)	Completed
Ph.D. (Completed/Ongoing)	Not Completed
Projects Carried out	-
Patents (Filed & Granted)	-
Technology Transfer	-
Research Publications (No.of papers published in National/International Journals/Conferences)	1.Complexity International Journal (CIJ) Volume 34, Issue 01, FEBRUARY 2021 Impact Factor (2020): 5.6 ISSN:1320-0682 CROP PROTECTION SYSTEM FROM WILD ANIMALS ATTACK USING WIRELESS TECHNOLOGY GARLANKI HARISH1, G BALA KISHORE2 2. Complexity International Journal (CIJ) Volume 34, Issue 01, FEBRUARY 2021 Impact Factor (2020): 5.6 ISSN:1320-0682 DELAY OPTIMIZED MODULAR ADDER DESIGN BASED ON THERMOMETER AND ONE-HOT CODING USING REVERSIBLE LOGIC LAKSHMI VEERA PAVANI EASWARI DEVI1, G BALA KISHORE2 3. Complexity International Journal (CIJ) Volume 34, Issue 01,
No. of Books published with details (Name of the book, Publisher with ISBN, year of publication, etc	FEBRUARY 2021 Impact Factor (2020): 5.6 ISSN:1320-0682 VLSI ARCHITECTURE OF MULTI STAAGE LINEAR FEEDBACK SHIFT REGISTER COUNTERS DECODING LOGIC FOR HIGH SPEED APPLICATIONS BATTHULA RAVITEJA1, G BALA KISHORE2 -